Distributed Algorithms

(Part 2)

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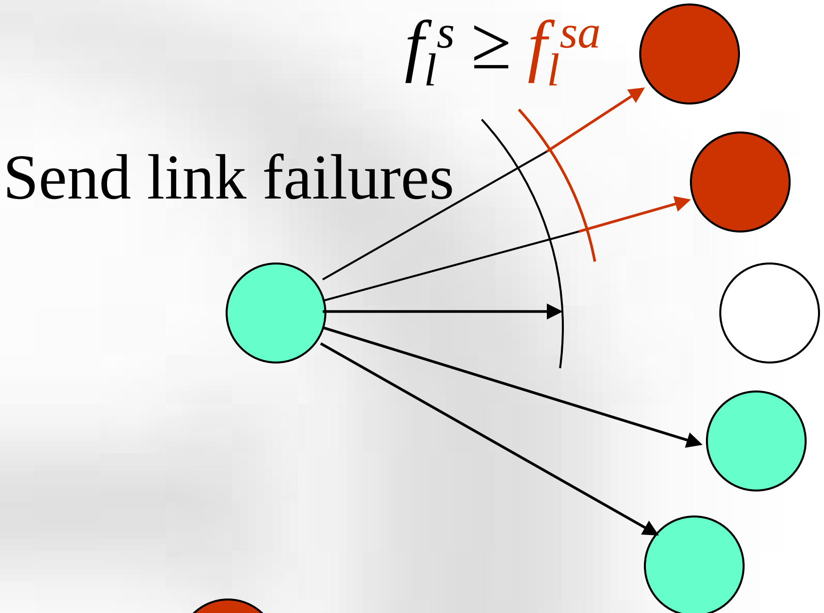
FAKULTÄT FÜR !NFORMATIK

Faculty of Informatics

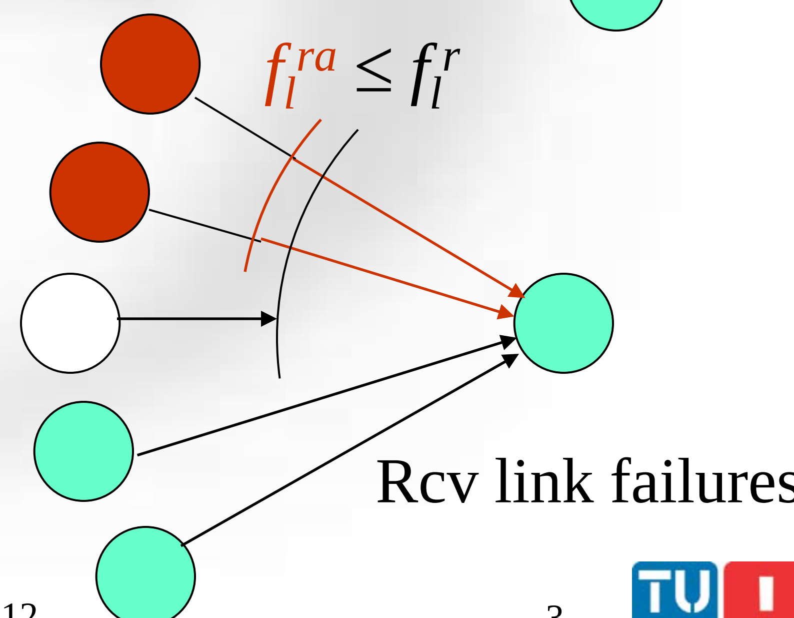
Food for Thoughts

Communcation Failures

- Link failure model:
  1. Distinguish send and receive link failures
  2. Distinguish omission and arbitrary link failures
  3. Indep. for every send/rec to/from all



- Known results:
  - $n > f_l^r + f_l^s$ necessary & sufficient for solving consensus with pure link omission failures
  - $n > f_l^r + f_l^{ra} + f_l^s + f_l^{sa}$ necessary & sufficient for solving consensus with link omission and arbitrary failures



Exercises

1. Find the smallest values for S,R,S',R',S'',R'' in the CB implem. below for arbitrary link failures ($f_l^r = f_l^{ra}$ and $f_l^s = f_l^{sa}$):

if got ($init,p_s,m_s$) from p_s
  $\rightarrow$ send ($echo,p_s,m_s$) to all [once]
if got ($echo,p_s,m_s$) from $Sf_l^{sa} + Rf_l^{ra} + f + 1$
  $\rightarrow$ send ($echo,p_s,m_s$) to all [once]
if got ($echo,p_s,m_s$) from $S'f_l^{sa}+R'f_l^{ra}+2f + 1$
  $\rightarrow$ call **accept**(p_s,m_s)

Required number of procs:

- $n \geq S''f_l^{sa}+R''f_l^{ra}+3f + 1$

Link failure lower bound:

- $n \geq f_l^r + f_l^{ra} + f_l^s + f_l^{sa}$

2. Find an „easy impossibility proof“ that shows that n=4 processors are not enough for solving consensus with $f_l^r = f_l^{ra} = f_l^s = f_l^{sa} = 1$ (and f =0)

Solution

Consistent BC with Comm. Failures (I)

Ulrich Schmid and Christof Fetzer. Randomized asynchronous consensus with imperfect communications. Technical Report 183/1-120, Department of Automation, Technische Universität Wien, January 2002. (Appeared in Proc. SRDS‘02).
http://wwwold.ecs.tuwien.ac.at/W2F/papers/SF02_byzTR.ps

if got $(init, p_s, m_s)$ from p_s

$\rightarrow$ send $(echo, p_s, m_s)$ to all [once]

if got $(echo, p_s, m_s)$ from $f_l^{sa} + f_l^{ra} + f + 1$

$\rightarrow$ send $(echo, p_s, m_s)$ to all [once]

if got $(echo, p_s, m_s)$ from $f_l^{sa} + 3f_l^{ra} + 2f + 1$

$\rightarrow$ call **accept**(p_s, m_s)

Fig. 2

Required number of procs:

- $n \geq 2f_l^{sa} + 4f_l^{ra} + 3f + 1$ (Thm. 2)

Link failure lower bound:

- $n \geq f_l^{r} + f_l^{ra} + f_l^{s} + f_l^{sa}$

Consistent BC with Comm. Failures (II)

The following follows right from the failure model (Lemma 1):

(1) Every correct processor p_i may receive at most $f_l^{ra} + f$ faulty echo msgs

(2) At most f_l^{sa} (correct) processors can emit echo, due to send link failures of p_s

(3) At most $2f_l^{ra} + f$ messages received by a correct processor by time t may not have been received at any other correct processor by time $t + \varepsilon$

Unforgeability:

- For a contradiction, suppose p_i calls **accept** by t+2d, so must have got $f_l^{sa}+3f_l^{ra}+2f+1$ echo msgs
- At most $f_l^{sa} + f_l^{ra} + f$ of these could originate from (1) and (2) → at least one (in fact, more) correct p_j must have emitted echo for good. This happens either
  - if p_j properly received init – which cannot happen as p_s did not call **bcast** by t
  - if p_j received $f_l^{sa} + f_l^{ra} + f + 1$ echo msgs itself, in which case we can repeat the argument above for p_j

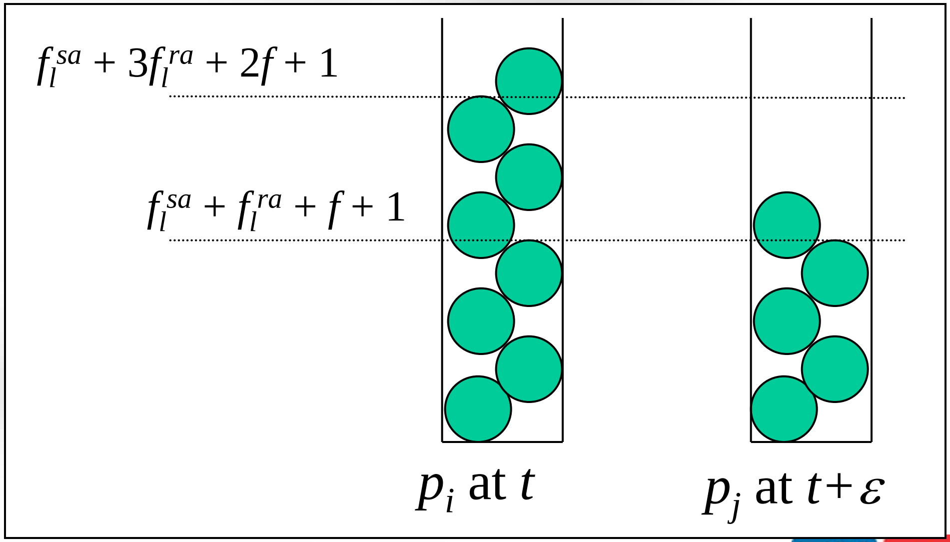
Consistent BC with Comm. Failures (III)

Correctness:

- Since p_s is correct, at least $n - f_l^{sa} - f \geq f_l^{sa} + 4f_l^{ra} + 2f + 1$ will get the init msg and emit echo by time $t+d+\varepsilon$
- Since every receiver could miss at most f_l^{ra} of these messages, at least $f_l^{s} + 3f_l^{ra} + 2f + 1$ are received by time $t+2(d+\varepsilon)$ → **accept** is triggered

Relay:

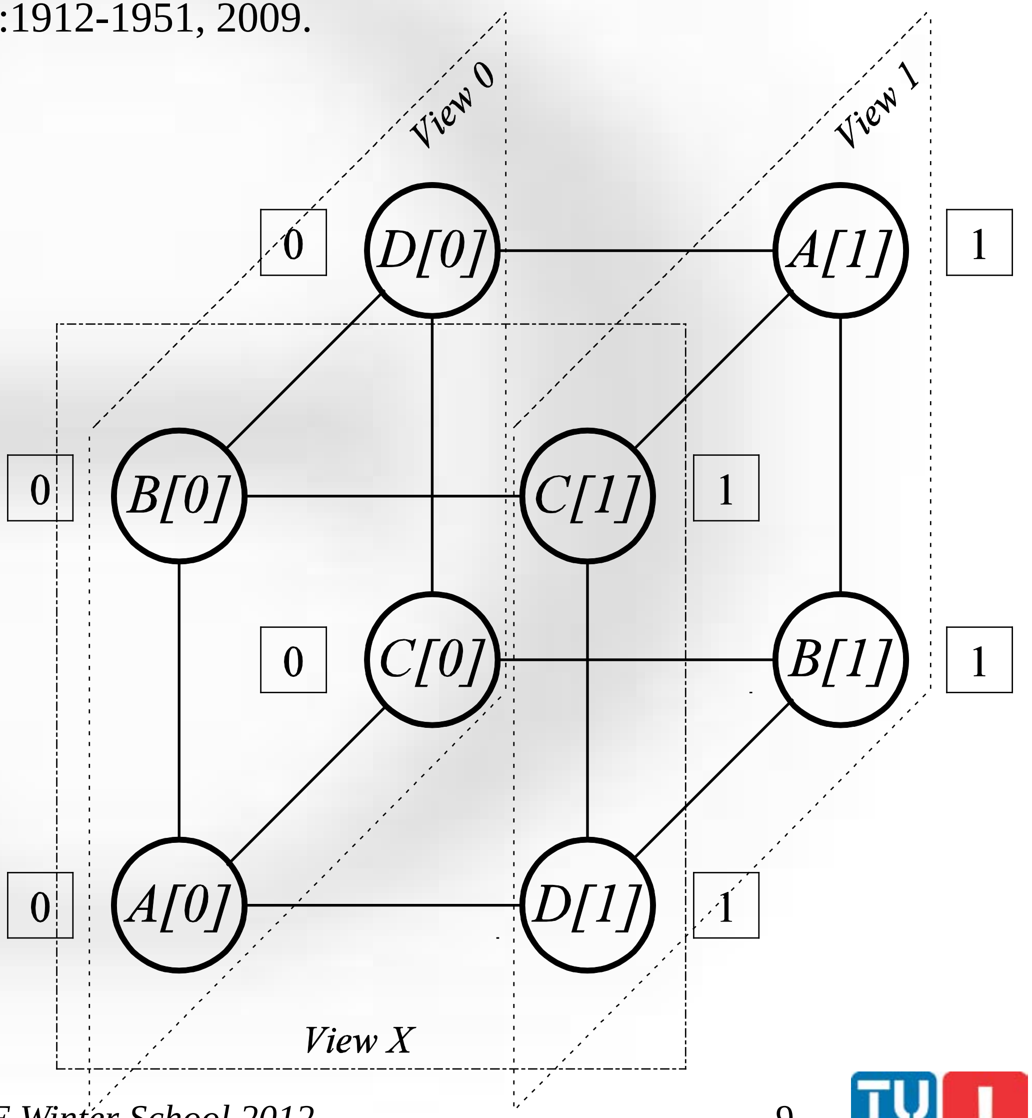
- By (3), at most $2f_l^{ra} + f$ of the echo messages available at p_i by t could be missing at p_j by $t + \varepsilon$
- $f_l^{sa} + f_l^{ra} + f + 1$ remain, so trigger emitting echo at p_j → continue as in original Relay-proof



Easy Impossibility Proof

Ulrich Schmid, Bettina Weiss, and Idit Keidar. Impossibility results and lower bounds for consensus under link failures. *SIAM Journal on Computing*, 38(5):1912-1951, 2009.

- Suppose correct algorithm $\mathcal{A}$ = (A,B,C,D) for (p_0,p_1,p_2,p_3) existed
- Consider this cube:
  - In View 0: Decision is 0 by Validity
  - In View 1: Decision is 1 by Validity
  - In View X: Violation of Agreement

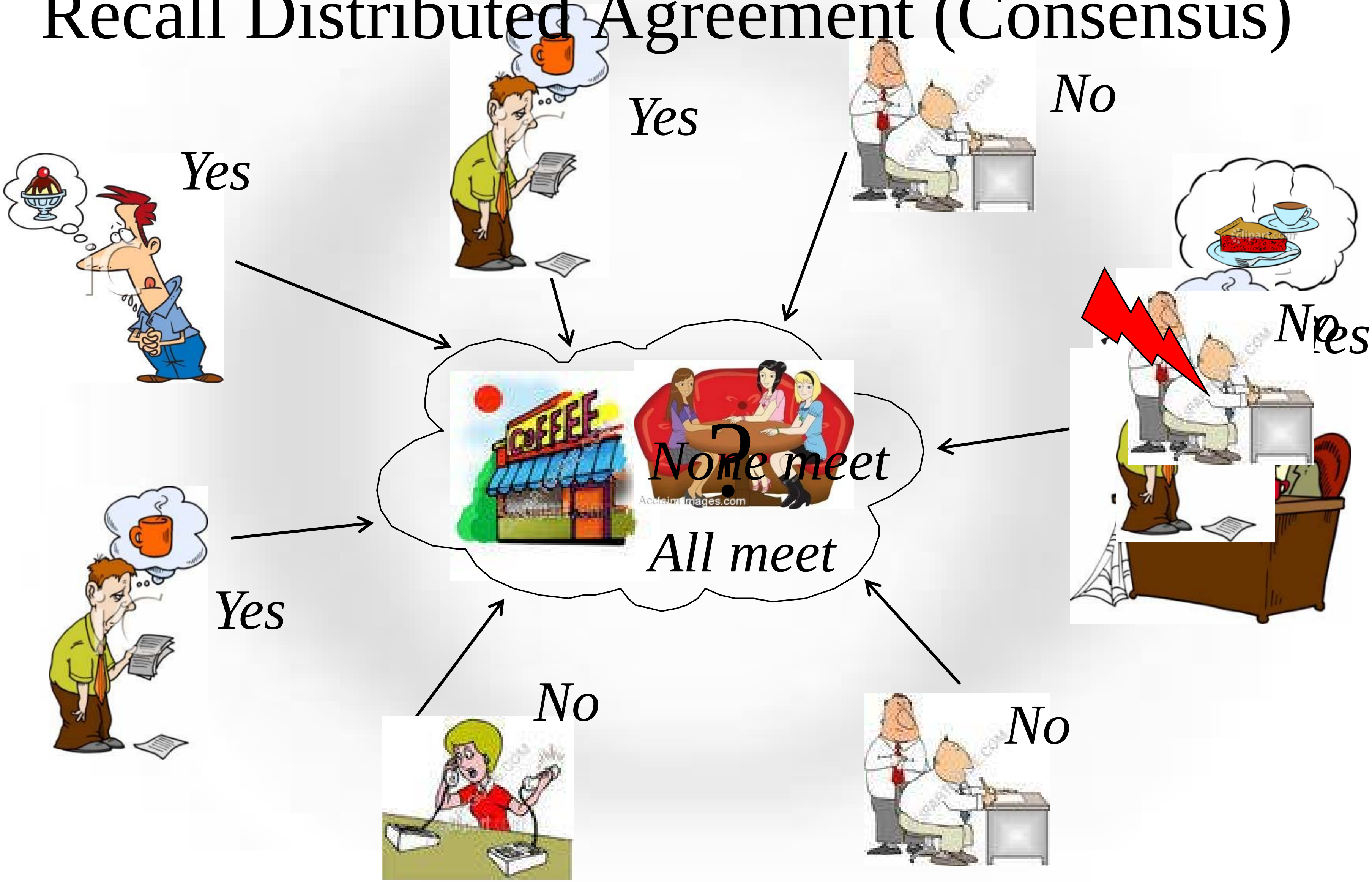


Content (Part 2)

- The Role of Synchrony Conditions:
  - Failure Detectors
  - Real-Time Clocks
- Partially Synchronous Models
  - Models supporting lock-step round simulations
  - Weaker partially synchronous models
- Distributed Real-Time Systems

The Role of Synchrony Conditions

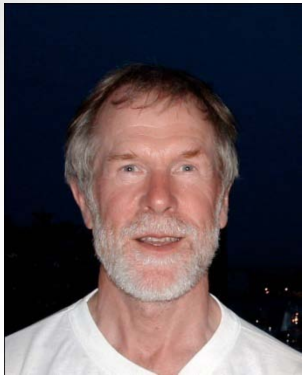
Recall Distributed Agreement (Consensus)



Consensus Impossibility (FLP)

Fischer, Lynch und Paterson [FLP85]:

"There is no deterministic algorithm for solving consensus in an asynchronous distributed system in the presence of a single crash failure."



Key problem:

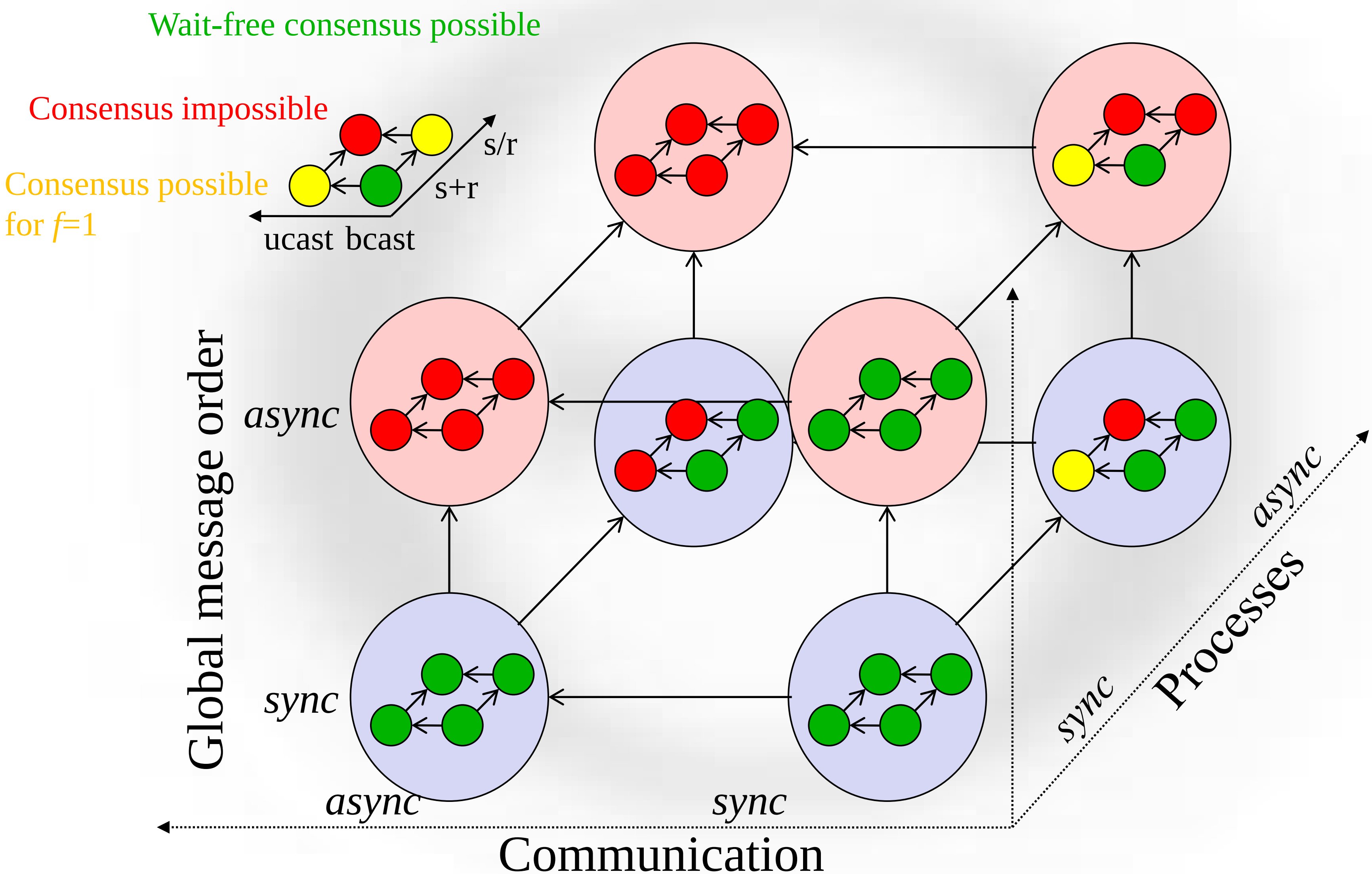
Distinguish slow from dead!

Consensus Solvability in ParSync [DDS87] (I)

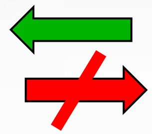
Dolev, Dwork and Stockmeyer investigated consensus solvability in Partially Synchronous Systems (ParSync), varying 5 **„synchrony handles“** :

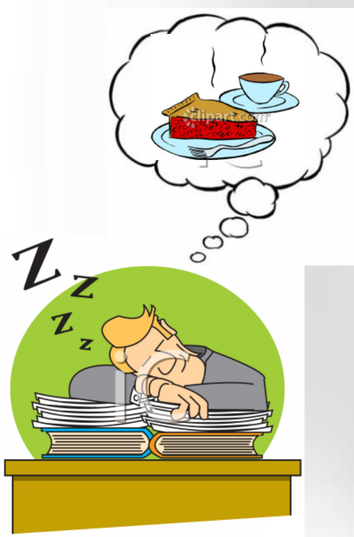
- Processors synchronous / asynchronous
- Communication synchronous / asynchronous
- Message order synchronous (system-wide consistent) / asynchronous (out-of-order)
- Send steps broadcast / unicast
- Computing steps atomic rec+send / separate rec, send

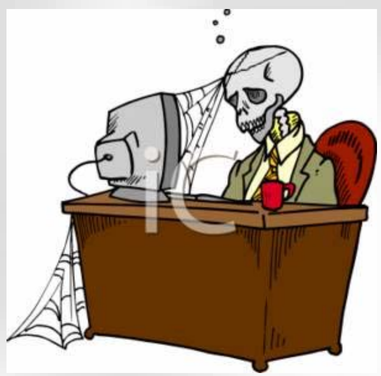
Consensus Solvability in ParSync [DDS87] (II)

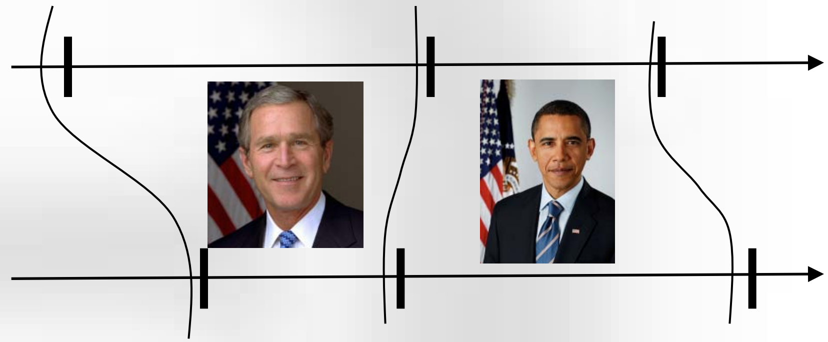


The Role of Synchrony Conditions

Enable failure detection  **Enforce event ordering**







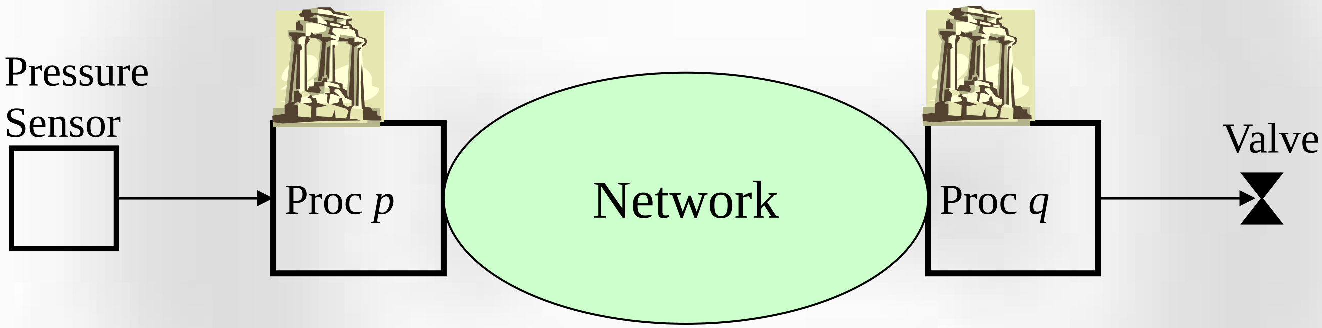
- Distinguish slow from dead

- Distinguish „old“ from „new“
- Ruling out existence of stale (in-transit) information
- Creating non-overlapping „phases of operation“ (rounds)

Failure Detectors

Failure Detectors [CT96] (I)

- Chandra & Toueg augmented purley asynchronous systems with (unreliable) failure detectors (FDs):



- Every processor owns a local FD module (an „**oracle**“ – we do not care about how it is implemented!)
- In every step [of a purely asynchronous algorithm], the FD can be queried for a hint about failures of other procs

Failure Detectors [CT96] (II)

-  make mistakes – the (time-free!) FD specification restricts the allowed mistakes of a FD
- FD hierarchy: A stronger FD specification implies
  - less allowed mistakes
  - more difficult problems to be solved using this FD
  - But: FD implementation more demanding/difficult
- Every problem *Pr* has a weakest FD *W:*
  - There is a purely asynchronous algorithm for solving *Pr* that uses *W*
  - Every FD that also allows to solve *Pr* can be transformed (via a purely asynchronous algorithm) to simulate *W*

Example Failure Detectors (I)

- Perfect failure detector P: Outputs suspect list
  - *Strong completeness*: Eventually, every process that crashes is permanently suspected by every correct process
  - *Strong accuracy*: No process is ever suspected bevor it crashes

- Eventually perfect failure detector ◊P:
  - *Strong completeness*
  - *Eventual strong accuracy*: There is a time after which correct processes are never suspected by correct processes

Example Failure Detectors (II)

- Eventually strong failure detector ◊S:
  - *Strong completeness*
  - *Eventual weak accuracy*: There is a time after which some correct process is never suspected by correct processes
- Leader oracle Ω: Outputs a single process ID
  - There is a time after which every not yet crashed process outputs the same correct process *p* (the „leader“)
- Both are weakest failure detectors for consensus (with majority of correct processes)

Consensus with ◊S: Rotating Coordinator

Task $T1$:

(1) $r_i \leftarrow 0$; $est_i \leftarrow v_i$;
(2) **while** $true$ **do**
(3) $c \leftarrow (r_i \bmod n) + 1$; $r_i \leftarrow r_i + 1$; % $1 \le r_i < +\infty$ %

———— Phase 1 of round r: from p_c to all ————

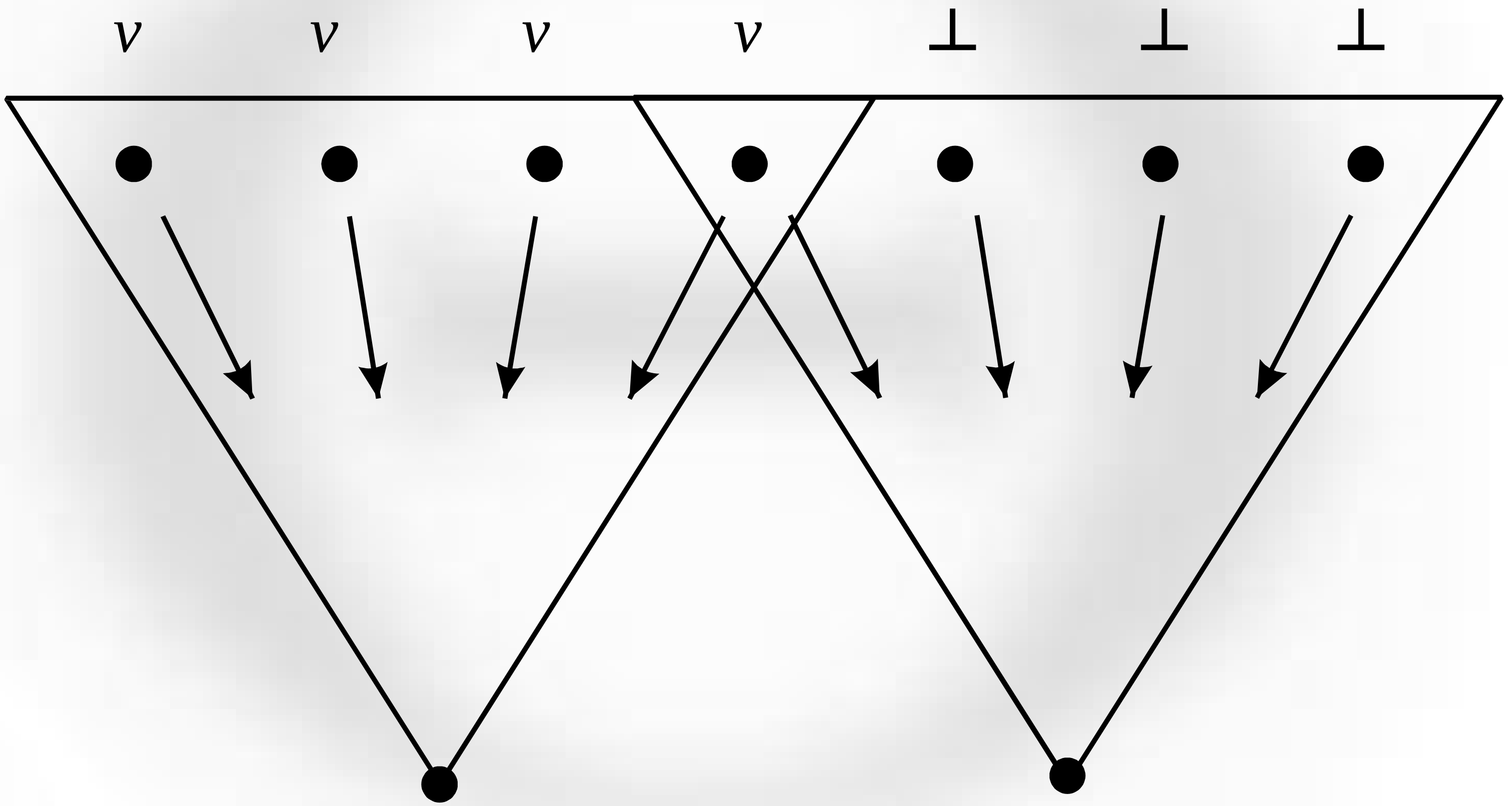
(4) **if** $(i = c)$ **then** *broadcast* PHASE1(r_i, est_i) **endif**;
(5) **wait until** (PHASE1(r_i, v) has been received from $p_c \vee c \in suspected_i$);
(6) **if** (PHASE1(r_i, v) received from p_c) **then** $aux_i \leftarrow v$ **else** $aux_i \leftarrow \perp$ **endif**;

———— Phase 2 of round r: from all to all ————

(7) *broadcast* PHASE2(r_i, aux_i);
(8) **wait until** (PHASE2 (r_i, aux) msgs have been received from a majority of proc.);
(9) **let** rec_i be the set of values received by p_i at line 8;
% We have $rec_i = \{v\}$, or $rec_i = \{v, \perp\}$, or $rec_i = \{\perp\}$ where $v = est_c$ %
(10) **case** $rec_i = \{v\}$ **then** $est_i \leftarrow v$; *broadcast* DECISION(est_i); **stop** $T1$
(11) $rec_i = \{v, \perp\}$ **then** $est_i \leftarrow v$
(12) $rec_i = \{\perp\}$ **then skip**
(13) **endcase**
(14) **endwhile**

Why Agreement? Intersecting Quorums

Intersecting Quorums:



n=7

f=3

p decides *v*

every *q* changes its estimate to *v*

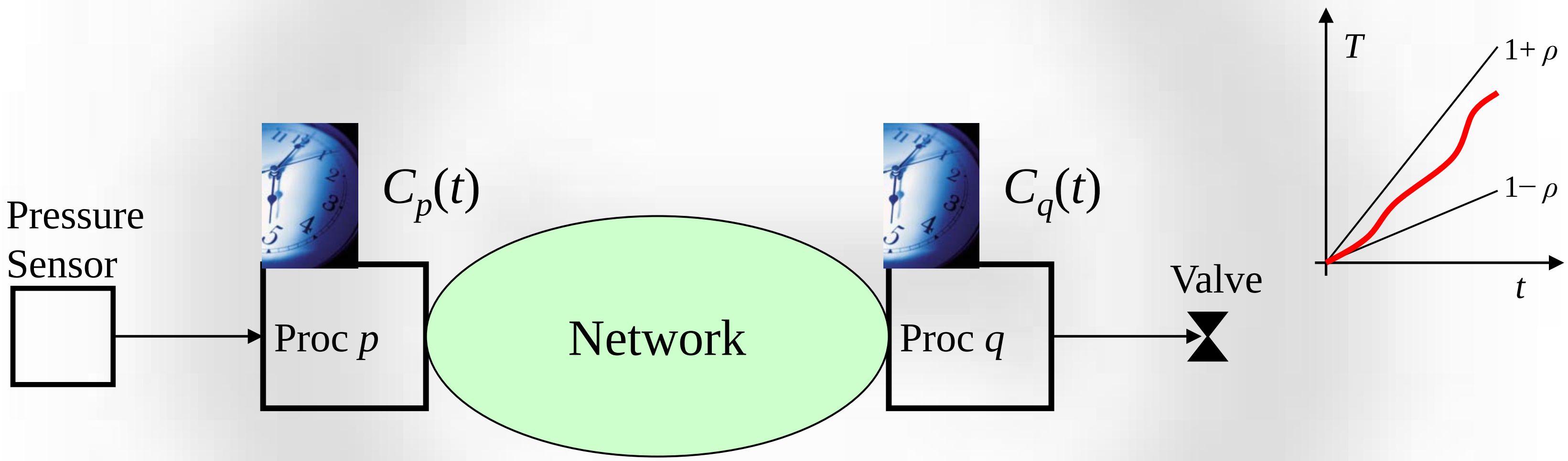
Implementability of FDs

- If we can implement a FD like Ω or ◊S, we can also implement consensus (for $n > 2f$)
- In a purely asynchronous system
  - it is impossible to solve consensus (FLP result)
  - it is hence also impossible to implement Ω or ◊S
- Back at key question: What needs to be added to an asynchronous system to make Ω or ◊S implementable?
  - Real-time constraints [ADFT04, …]
  - Order constraints [MMR03, …]
  - ???

Real-Time Clocks

Distributed Systems with RT Clocks

- Equip every processor p with a local RT clock $C_p(t)$



- Small clock drift ρ → local clocks progress approximately as real-time, with clock rate $\in [1-\rho, 1+\rho]$
- End-to-end delay bounds $[\tau^-, \tau^+]$, *a priori* known

The Role of Real-Time

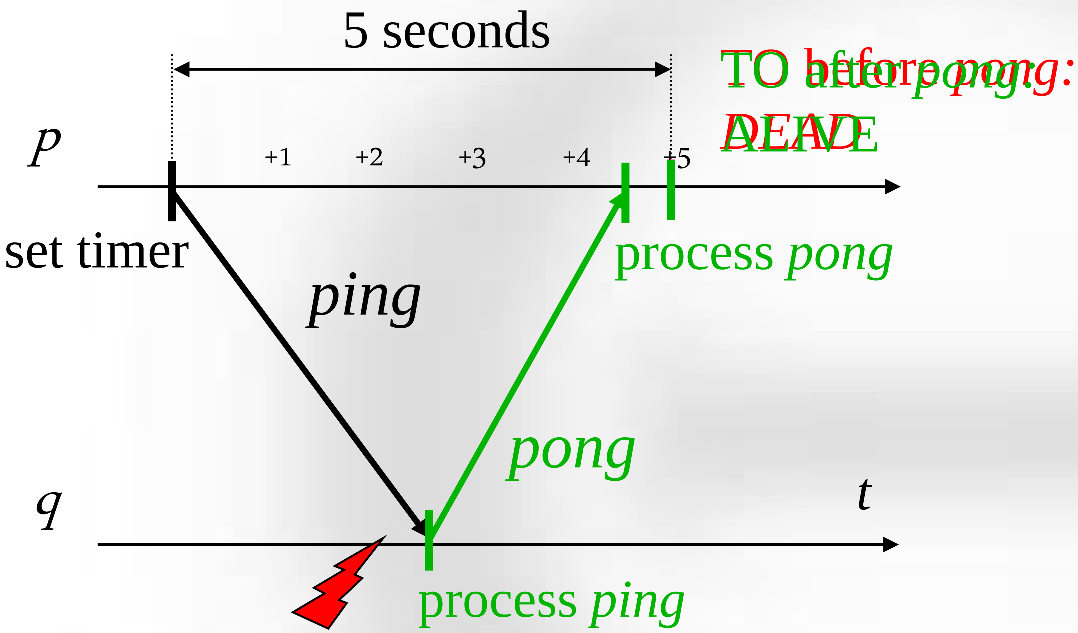
- Real-time clocks enable both:

Failure detection

Event ordering

- [Show later: Real-time clocks are not the only way …]

Failure Detection: Timeout using RT Clock



status = do_roundtrip(q)
{ send *ping* to q
TO := $C_p(t)$ + 5 seconds
wait until $C_p(t)$ = TO
if *pong* did not arrive **then**
return DEAD
else
return ALIVE
}

p can reliably detect whether q has been alive recently, if

- the end-to-end delays are at most $\tau^+ = 2.5$ seconds
- τ^+ is known a priori [at coding time]

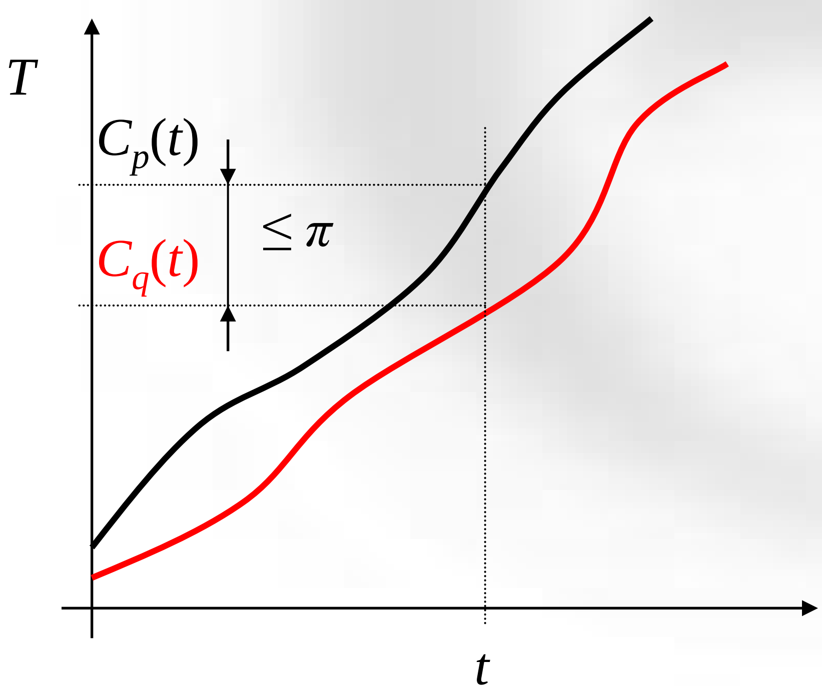
Event Ordering: Via Clock Synchronization

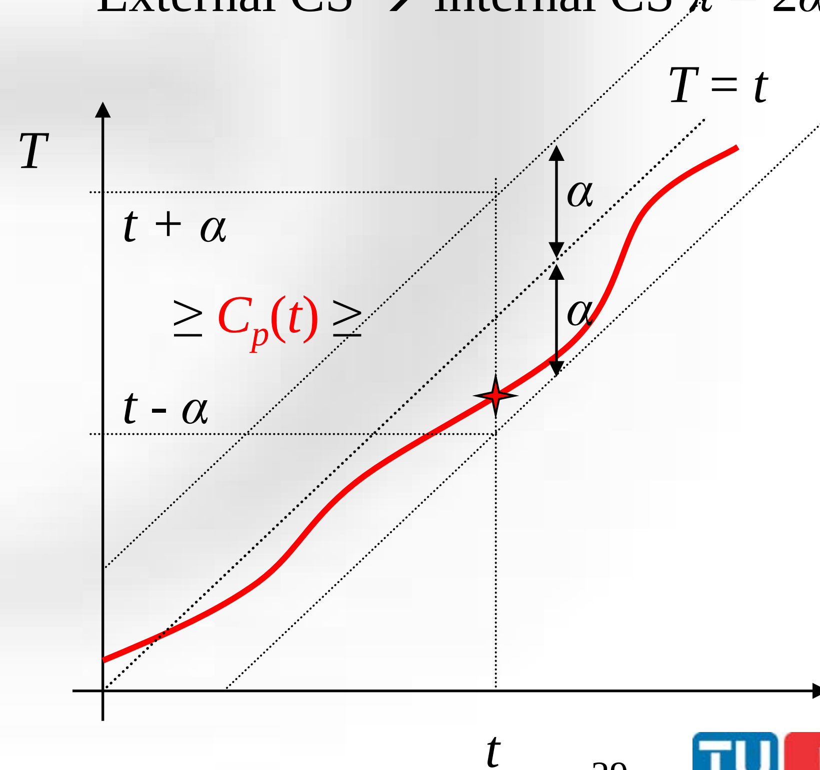
Internal CS:

- Precision $|C_p(t) - C_q(t)| \le \pi$
- Progress like RT (small drift ρ)
- CS-Alg must periodically resynchronize

External CS:

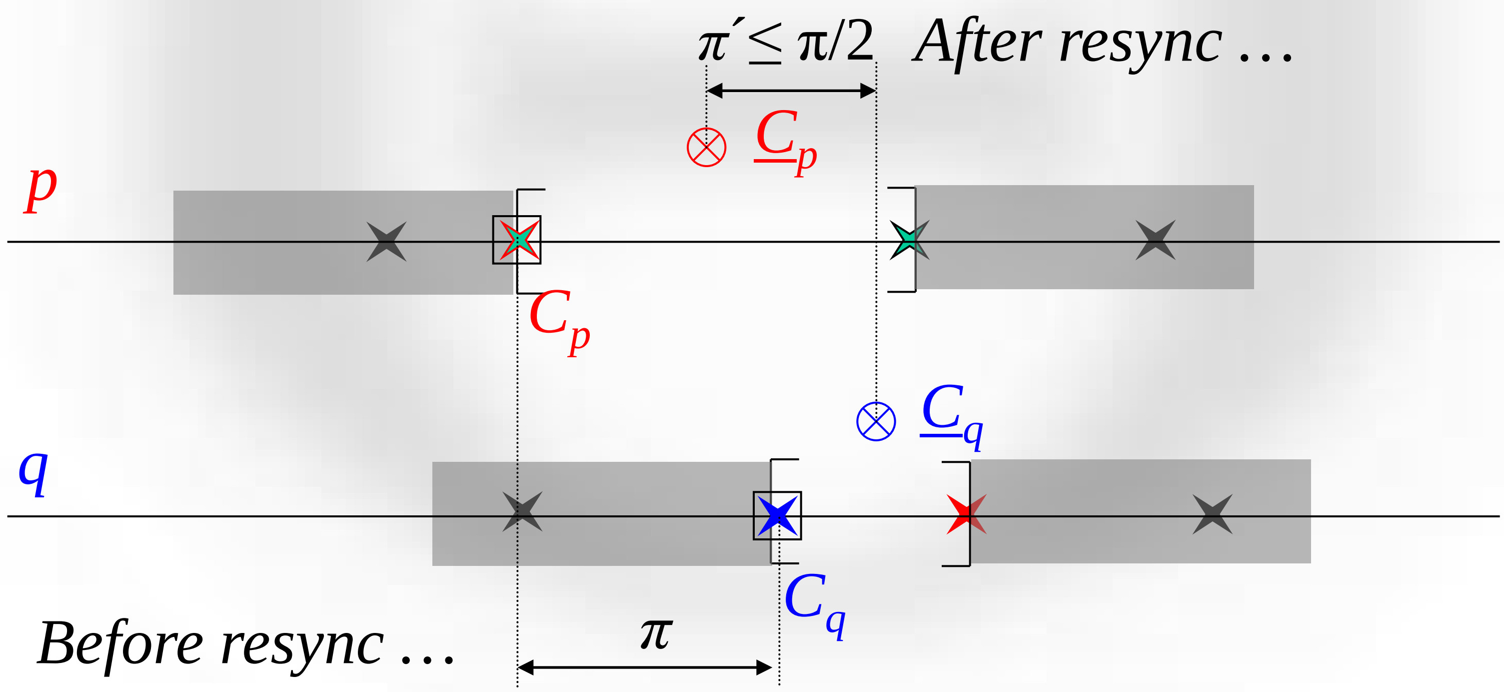
- Accuracy $|C_p(t) - t| \le \alpha$
- CS-Alg needs access to RT
- External CS → internal CS $\pi = 2\alpha$



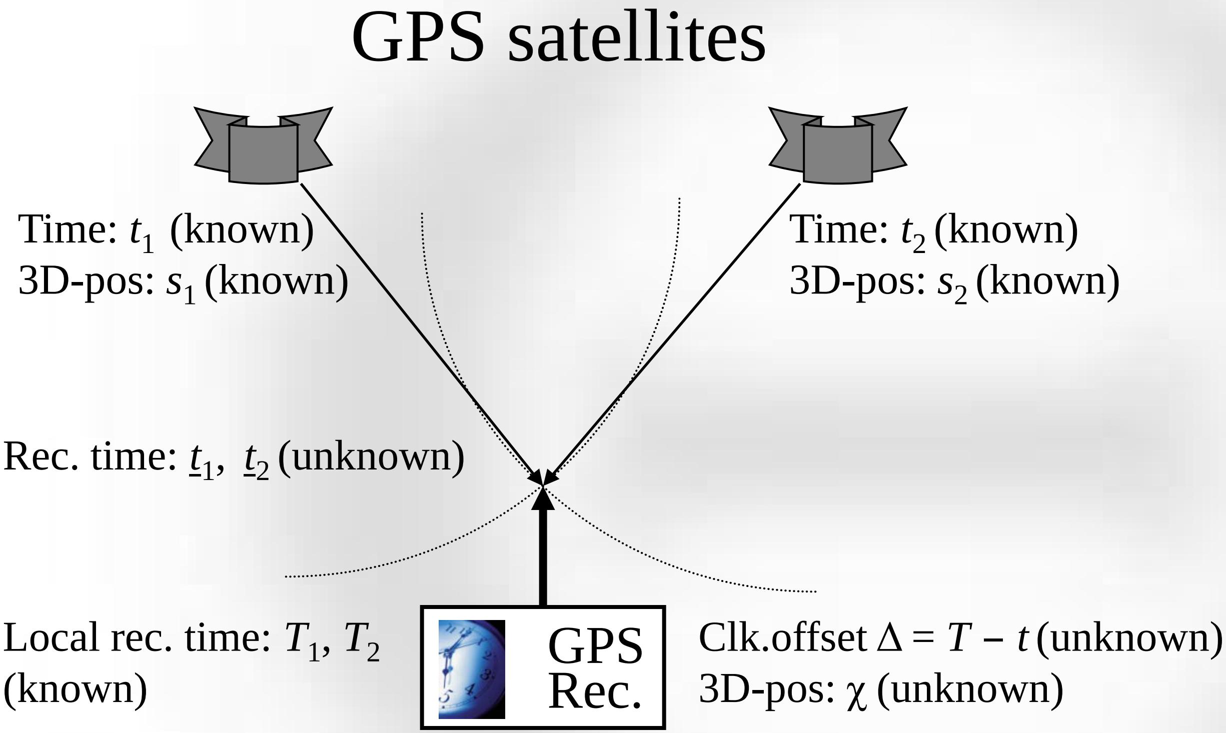


FT Midpoint Internal CS-Alg [LWL88]

- A priori bounded $[\tau^-, \tau^+]$ allows to estimate all remote clocks
- Discard f largest and f smallest clock readings (could be faulty)
- Set local clock to midpoint of remaining interval



Global Positioning System (GPS)



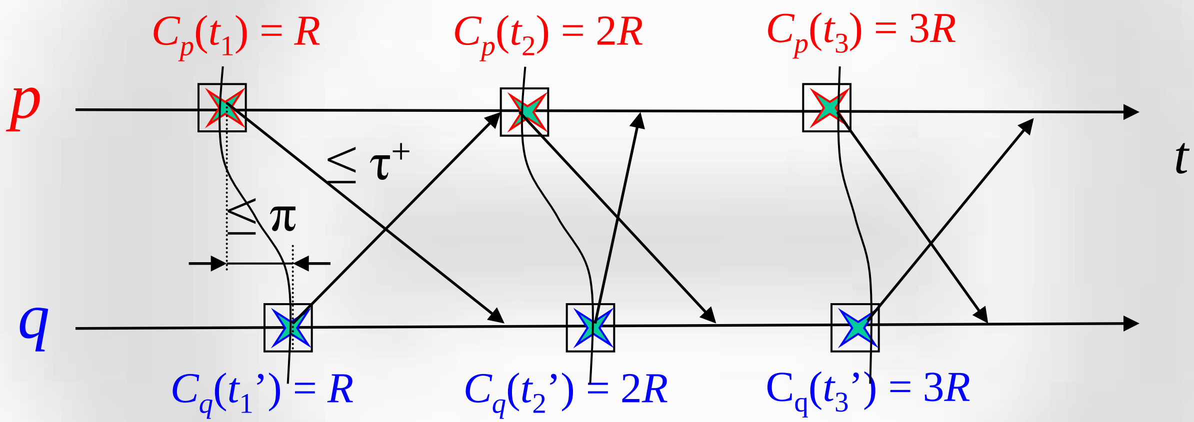
- Satellite clocks synchronized to USNO atomic master clock
- GPS-Receiver solves system of equations

$$t_i + |\chi - s_i|/c + \Delta = T_i$$

- 4 satellites required to determine $\chi = (x, y, z)$ and Δ
- 1 satellite sufficient for Δ if χ is already known

Why are Synchronized Clocks Useful?

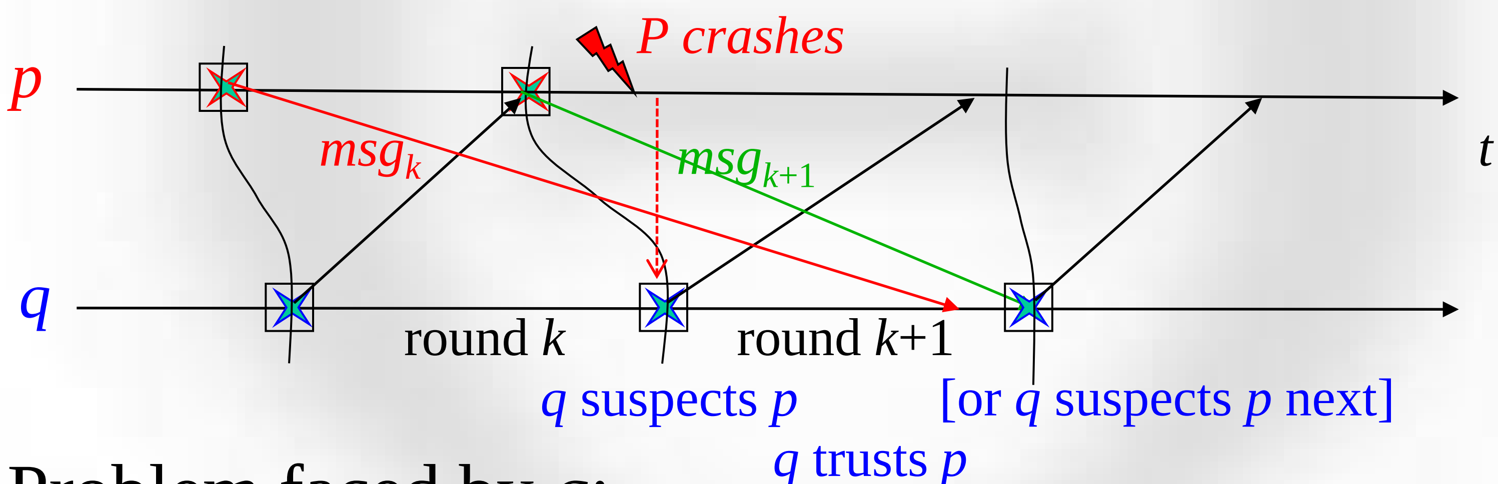
- Synchronized clocks allow to simulate communication-closed lock-step rounds via clock time [NT93]:



- **Only requirement: $R \geq \tau^+ + \pi$ holds!**
- Lock-step rounds ⟹ perfect failure detection at end of rounds

Perfect FD $\not\Rightarrow$ Lock-Step Round Simulation

- Attempt round simulation at *p*: Waiting for either
  - arrival of round message from *q*, or
  - *p*‘s instance of P suspects *q*



- Problem faced by *q*:
  - msg_k not received in round *k*, although *p* alive after round *k*
  - *q* even receives msg_{k+1} in round *k*+1 in this example

Using RT Clocks: Deficiencies

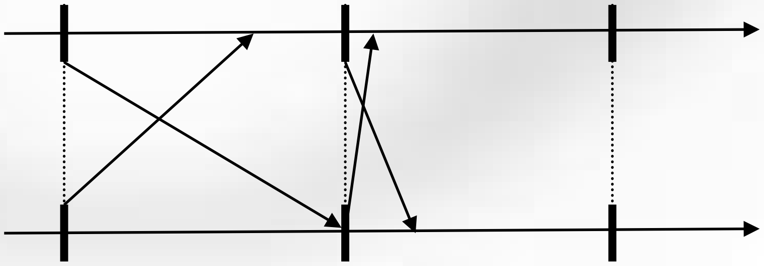
- Algorithms like do_roundtrip(.) have system-dependent time values (unit „seconds“) in their code / variables → not easily portable to e.g. faster hardware
- Fail-operational systems might tolerate occasional loss of timeliness properties – but never of safety properties
- Unfortunately:
  - Safety properties like agreement typically rely on the reliable operation of do_roundtrip(.) and similar primitives
  - End-to-end delay bounds τ^+ that always hold are difficult to determine in real systems

➢ Try to relax timing assumptions in ParSync models …

Partially Synchronous Models

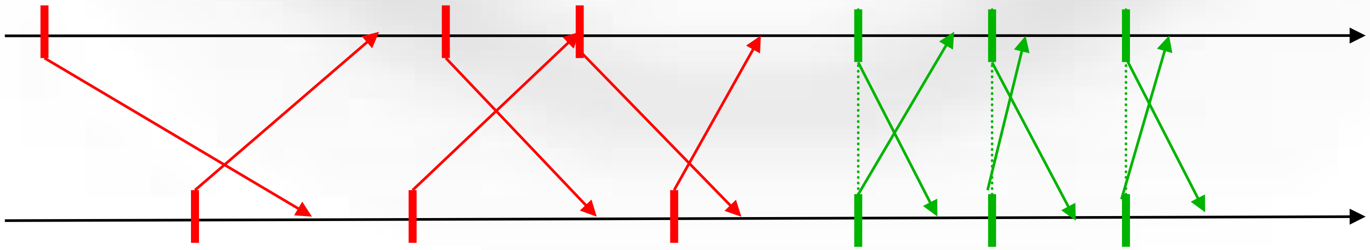
Recall: Synchronous Model

- „The“ classic model
  - Transmission delay bound τ^+
  - Computing step time bound μ^+
  - Bounded-drift local clocks available
- Allows (Byzantine-tolerant) implementation of
  - Internal clock synchronization
  - Lock-step rounds
  - etc.



The Timed Asynchronous Model

- Cristian & Fetzer [CF99]:
  - Alternating bad and good periods:
    - Transmission delay bound τ^+
    - Computing step time bound μ^+
  - Bounded-drift local RT clocks available
  - Local clocks allow to detect good/bad periods → TA algorithms are always safe and live in good periods
- TA algorithms allow to implement (non-Byzantine) fail-aware services, including eventual lock-step rounds



Classic Partially Synchronous Models (I)

- „The" classic ParSync models
  Dolev, Dwork & Stockmeyer [DDS87]
  Dwork, Lynch & Stockmeyer [DLS88]
  Attiya, Dwork, Lynch & Stockmeyer [ADLS94]
- Semi-synchronous model by Ponzio & Strong [PS92]
- Common system parameters:
  - Bounded processor speed ratio $\Phi = \mu^+/\mu^-$
  - Transmission delay bound Δ
- Archimedean model by Vitanyi [Vit84]
  - Bounded speed ratio $S = \tau^+/\mu^-$

Classic Partially Synchronous Models (II)

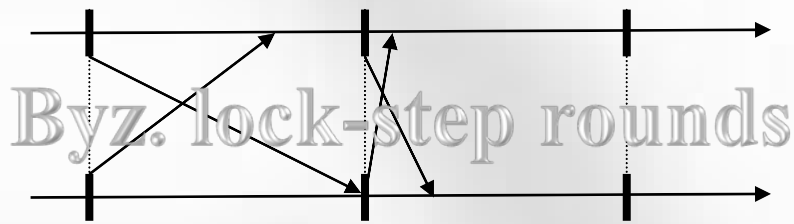
Processes can locally time-out messages:

- The classic ParSync models [DDS87, DLS88] and [ADLS94] assume
  - Δ given in multiples of (unknown) minimal computing step time μ^- [hence $\tau^+ = \Delta \cdot \mu^-$ real-time seconds]
  - spin loop counting f(Φ,Δ) steps allows to time-out messages [implements local clock with real-time rate $\in [1/\Phi,1]$]
- Archimedean model [Vit84] also allows to time-out messages via spin-loop for *S* steps
- Semi-synchonous model [PS92] assumes
  - $\Delta = \tau^+$ given in real-time seconds
  - bounded-drift local RT clocks available for timing-out messages

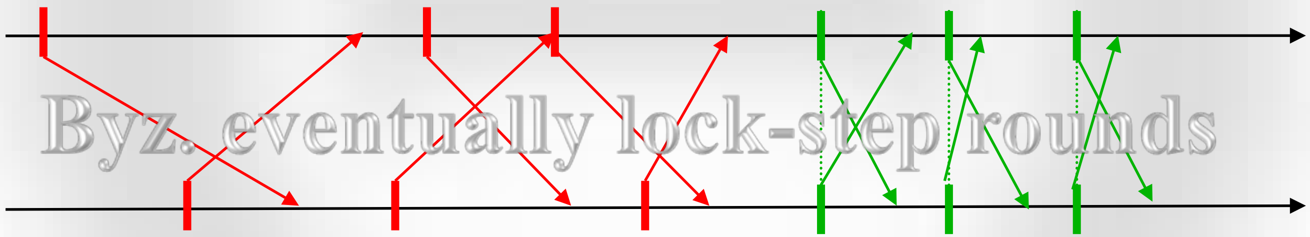
Classic Partially Synchronous Models (III)

Variants of ParSync models: System parameters (Δ, Φ)

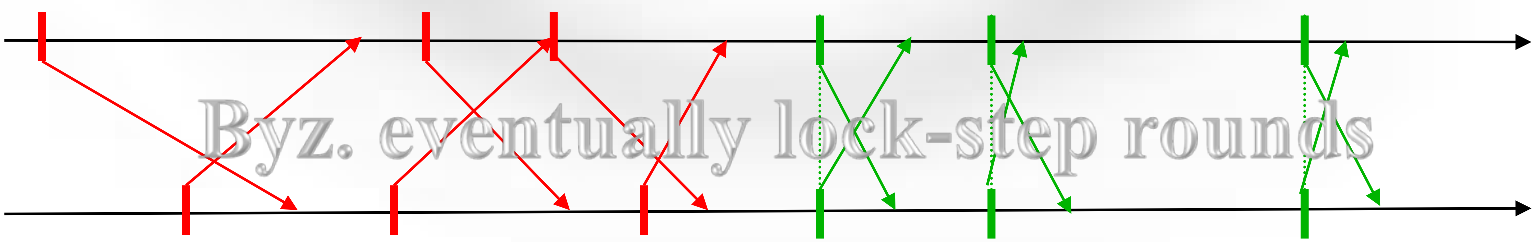
1. known and hold
   from the beginning



2. known and hold from unknown global stabilization time (GST) on



3. unknown and hold from the beginning / from GST on:
   Learn (Δ, Φ), by continuously increasing estimate values



Time-Free Message-Timeout in ParSync ?

- Implementation of do_roundtrip(p) in the ParSync models of [DLS88] or [Vit85]:

```
{  send ping to p
   for i=1 to x do no-op          /* x=f(Δ, Φ) resp. x=f(s) is
                                              dimensionless! */
   if pong did not arrive then
          return DEAD
   else
          return ALIVE
}
```

- But: No obvious correlation between processor step times and message delays → not really time-free …

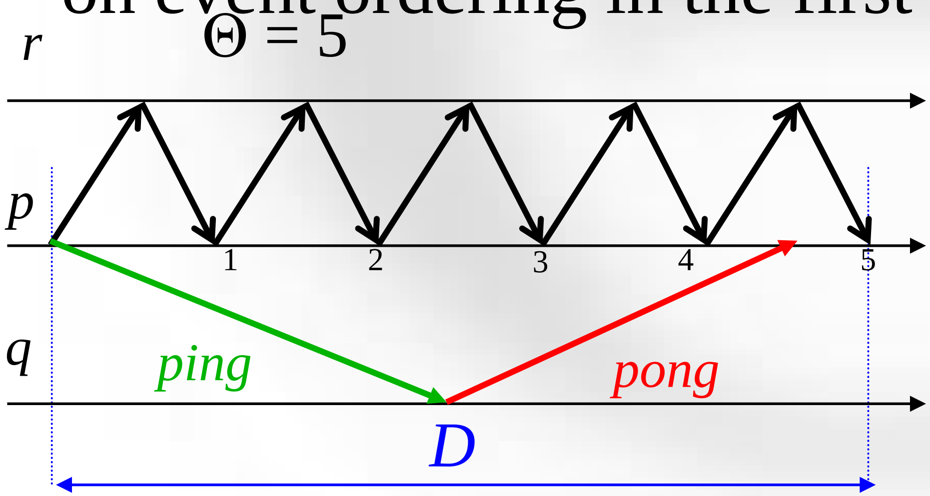
The Θ/ABC-Model

In classic ParSync model:

- only less than Θ roundtrips can occur during any single round-trip
- Timing assumptions are primarily used for ordering events
- Is it possible to define a time-free ParSync model based on event ordering in the first place?

For example: Assume that:

- Actual duration (D) irrelevant

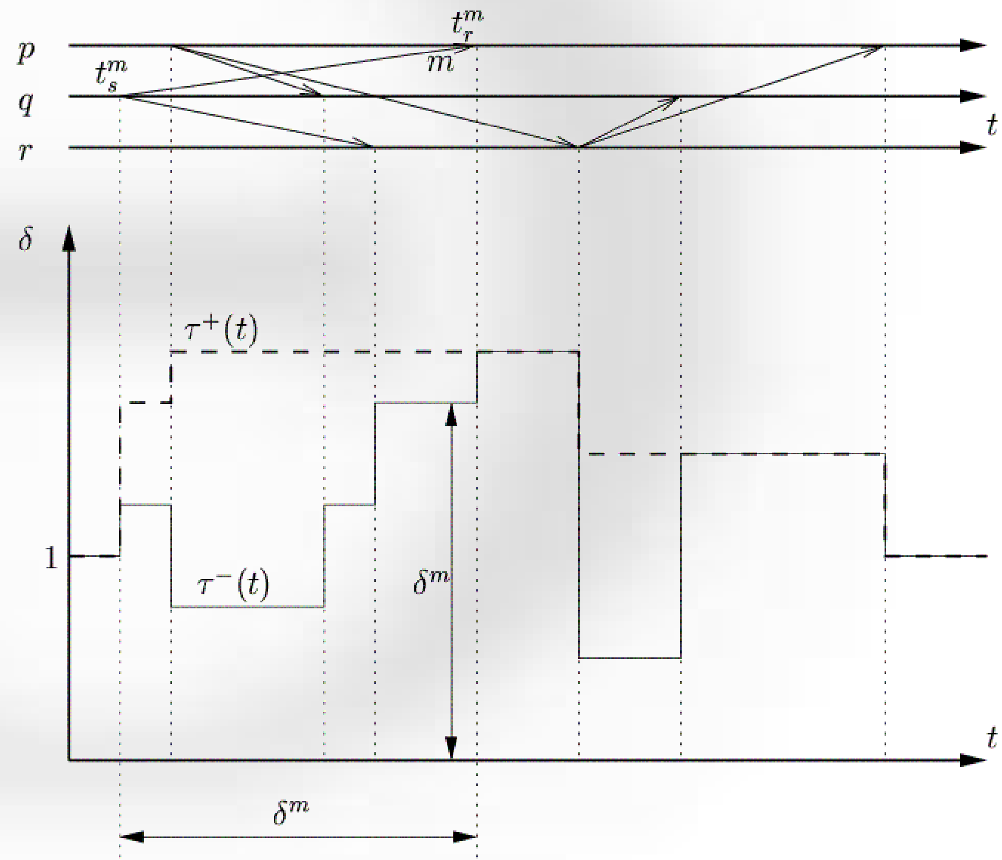



```
status = do_roundtrip(q)
{   send ping to q
    for i=1 to Θ do
    begin
       send delay_ping(i) to r
       wait for delay_pong(i) from r
    end
    if pong did not arrive then
           return DEAD
    else
           return ALIVE
}
```

The Θ-Model: Bounded E-t-E Delay Ratio

LeLann & Schmid [LS03], Widder & Schmid [WS09]

- End-to-end delays of all messages in transit at t
  - minimum $\tau^{-}(t)$
  - maximum $\tau^{+}(t)$
- $\tau^{+}(t)$ and $\tau^{-}(t)$ may vary arbitrarily with time, but:
- Ratio $\tau^{+}(t)/\tau^{-}(t)$ bounded by [known or even unknown] system parameter Θ



Byzantine FT Clock Sync in the Θ-Model

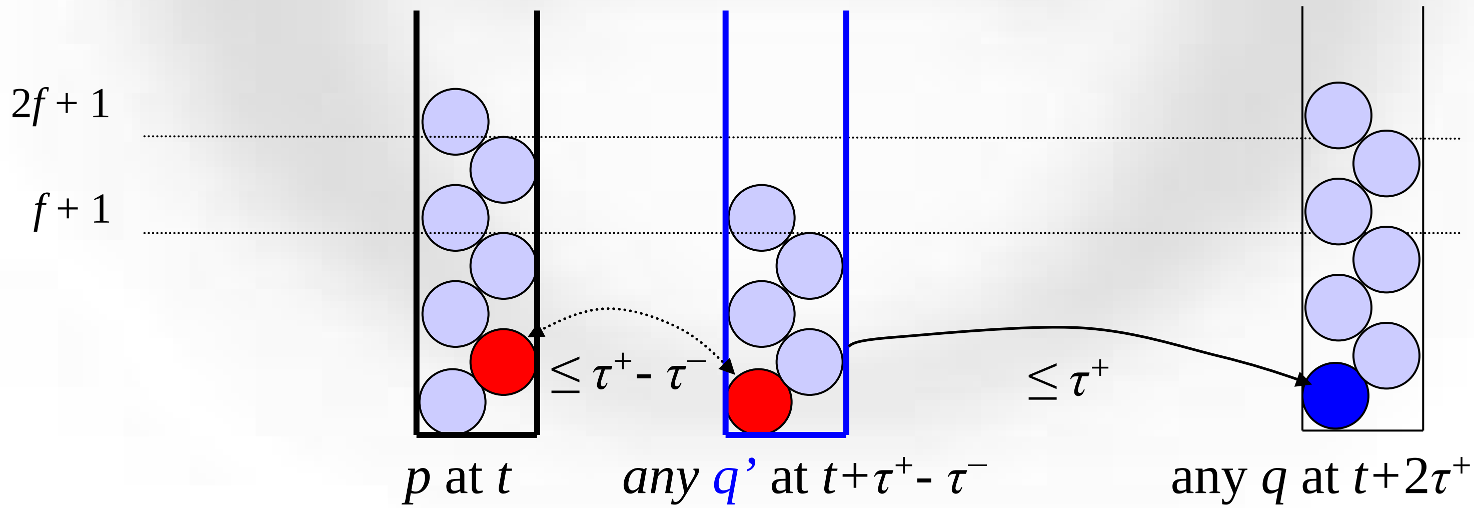
On init
→ send *tick*(0) to all; C := 0;
If got *tick*(l) from f +1 nodes **and** l > C
→ send *tick*(C+1),…, *tick*(l) to all;
C := l;
If got *tick*(C) from 2f +1 nodes
→ send *tick*(C+1) to all;
C := C+1;

For $n \geq 3f + 1$ with up to f Byz. failures:

- Suppose p sends *tick*(C+1) at time t
- Then, q also sends *tick*(C+1) by time $t + 2\tau^+ - \tau^-$

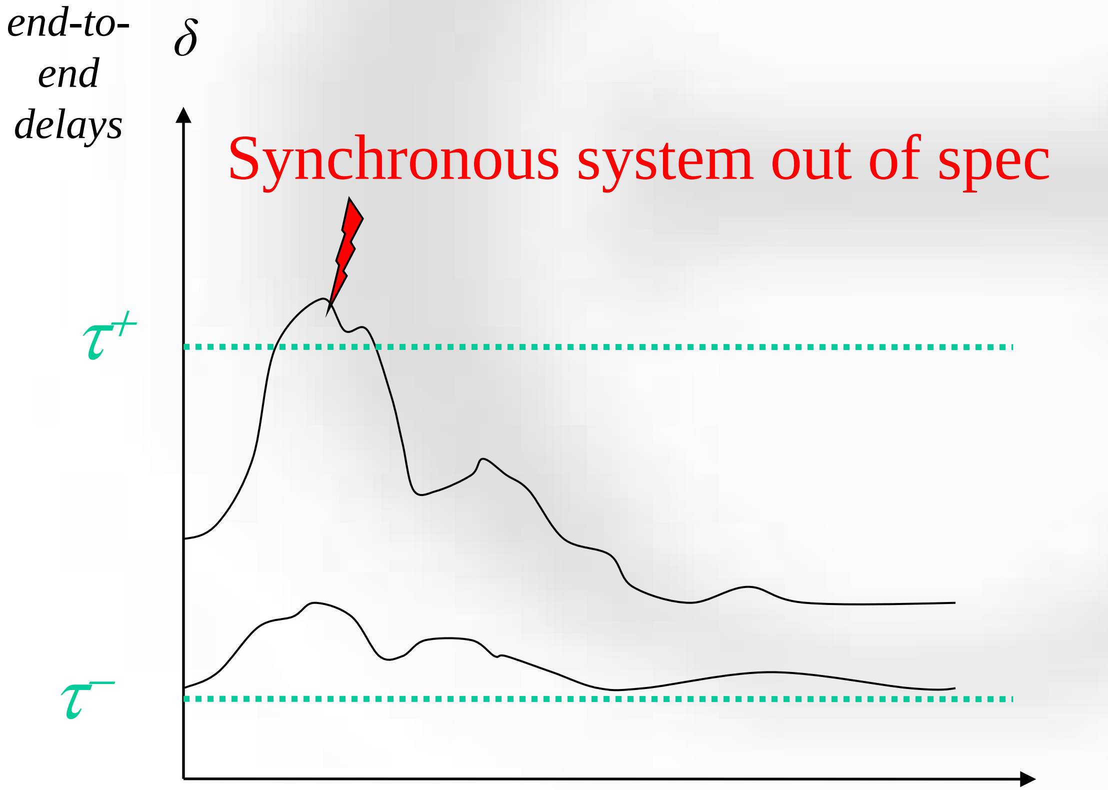
\+ Fastest tick-frequency of any p: $1/\tau^-$

⇒ Clock ticks occur approximately synchronously, with precision $\pi(\Theta)$



Correlation → Coverage Expansion

- Given some bound τ^+ and τ^- assumed during system design (as used in synchronous systems), compute $\Theta = \tau^+ / \tau^-$
- Unanticipated overload: $\tau^+(t) > \tau^+$ — if $\tau^+(t) \leq \Theta\tau^-(t)$, however,



Θ-system still OK

Note:

- $\tau^+(t) = \tau^+ + \alpha(t)$
- $\tau^-(t) = \tau^- + \alpha(t)/\Theta$
  sufficient for Θ to hold!

Shortcomings Θ-Model

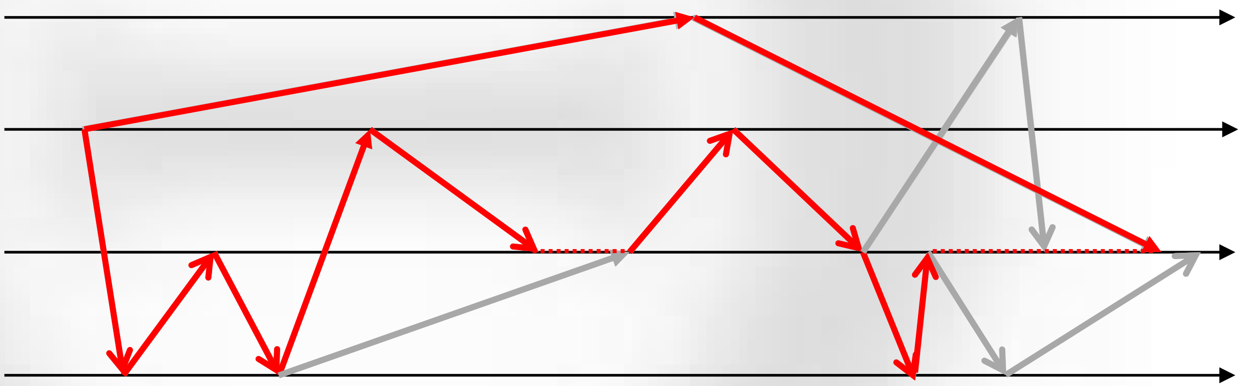
- Correlation between slow and fast messages need not exist for all messages
  - Some very fast messages [even $\tau^- = 0$] may be in transit somewhere in the system during a slow message
  - Correlation and hence coverage expansion does not exist in such cases
- Need a more relaxed definition of the relation between slow and fast messages
  - All that is actually needed is to constrain the number of fast messages during a slow one
  - No need for a correlation of unrelated messages, and at every point in time t

The Asynchronous Bounded Cycle Model

Robinson & Schmid [RS08]

- The ABC Model just bounds the ratio of the **number** of forward and backward-oriented messages in cycles

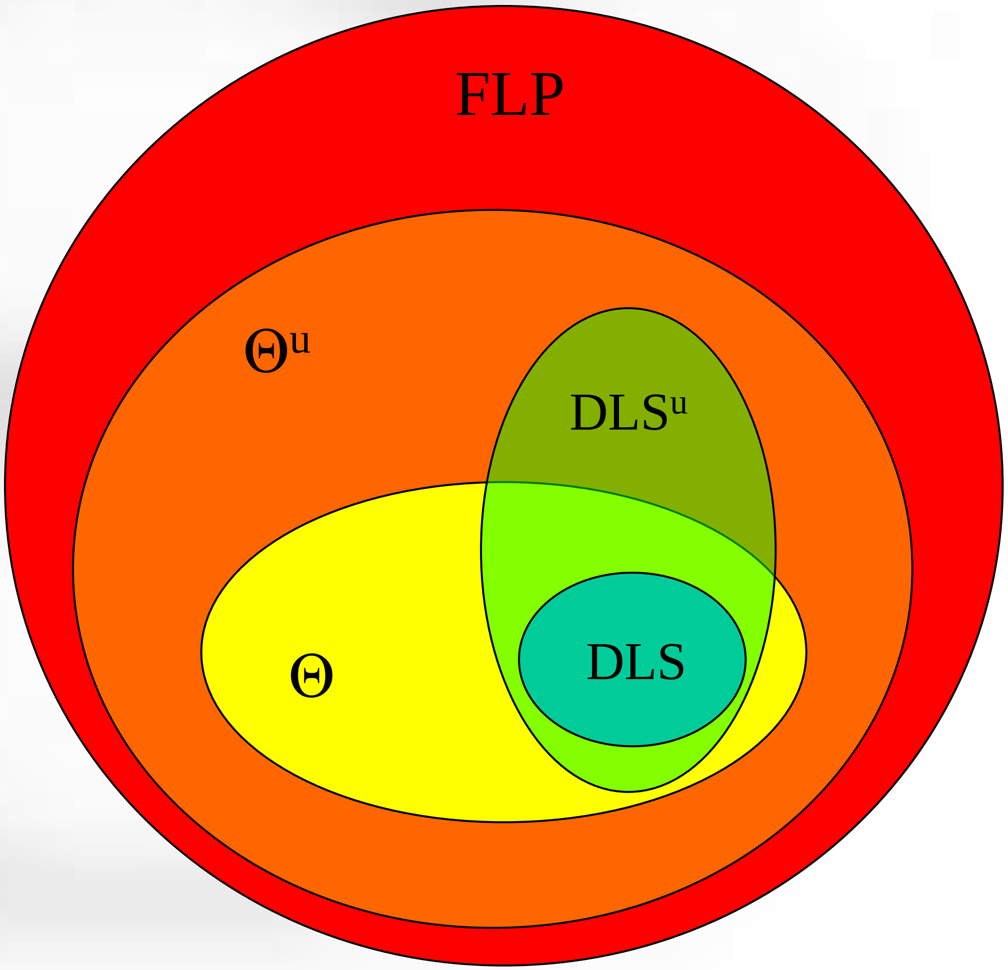
- Example: $\Theta = 4.5$
- 2 consecutive „slow“ messages
- Cycle with 9 enclosed „fast“ messages
- No larger cycles allowed



- No implicit or explicit reference to real-time
  - ✓ Messages with $\tau^{-}(t) = 0$ allowed
  - ✓ No need to relate independent messages in the system
  - ✓ **We proved: Any Θ-algorithm works correctly in the ABC model**

Partial Order of ParSync Models

- DLS … [DLS88] with known Δ, Φ
- Θ … ABC/Θ-Model with known Θ
- DLS^u … [DLS88] with unknown Δ, Φ
- Θ^u … ABC/Θ-Model with unknown Θ
- FLP … FLP-Model



Even Weaker ParSync Models?

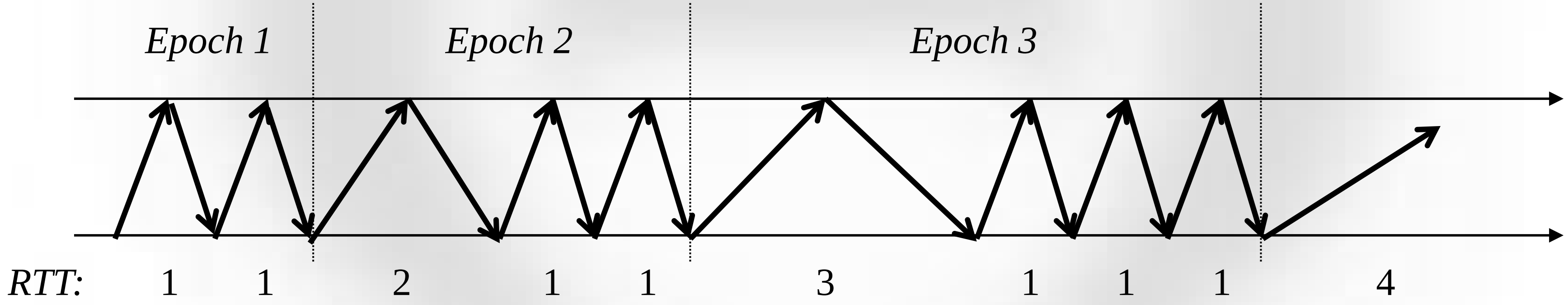
- All the ParSync Models seen so far allow to build
  - lock-step rounds, or at least
  - eventual lock-step rounds
- Solving consensus is easy here.
- We know that lock-step rounds are stronger than failure detectors that are sufficient for solving consensus:
  - Perfect failure detector P
  - Leader oracle Ω
- Are there weaker ParSync models where only such FDs can be implemented?

Weaker Partially Synchronous Models

Finite Average Roundtrip-Time Model (I)

Fetzer, Schmid and Süsskraut [FSS04]

- Asynchronous system with crash failures
- Unknown lower bound μ^- for computing step time
- Unknown average round-trip time bounds $\lim_{n\to\infty} \frac{1}{n}\sum_{k=1}^{n} RTT(k) < \infty$



- $RTT(k)$ and hence τ^+ unbounded, yet
- Average after n „Epochs“ is $$\frac{n(n+1)}{n(n+1)-(n-1)n/2} = 2\cdot\frac{n^2+n}{n^2+3n} < \infty$$

Finite Average Roundtrip-Time Model (II)

- The FAR model assumptions
  - do not allow to implement lock-step rounds
  - do allow to implement the eventually perfect FD P
  - can solve consensus if $n > 2f$
- Key ideas for P implementation:
  - Implement weak local clock [via spin-loop] for timing-out messages
  - Time-out roundtrips using adaptive timeout value TV
    - If fast RT occurs [before TO]: Increase TV, to prepare for future slow RTs
    - If slow RT occurs [after TO]: (Could) decrease TV, since fast RTs must eventually follow due to finite average RTT

Weak Timely Link Models (I)

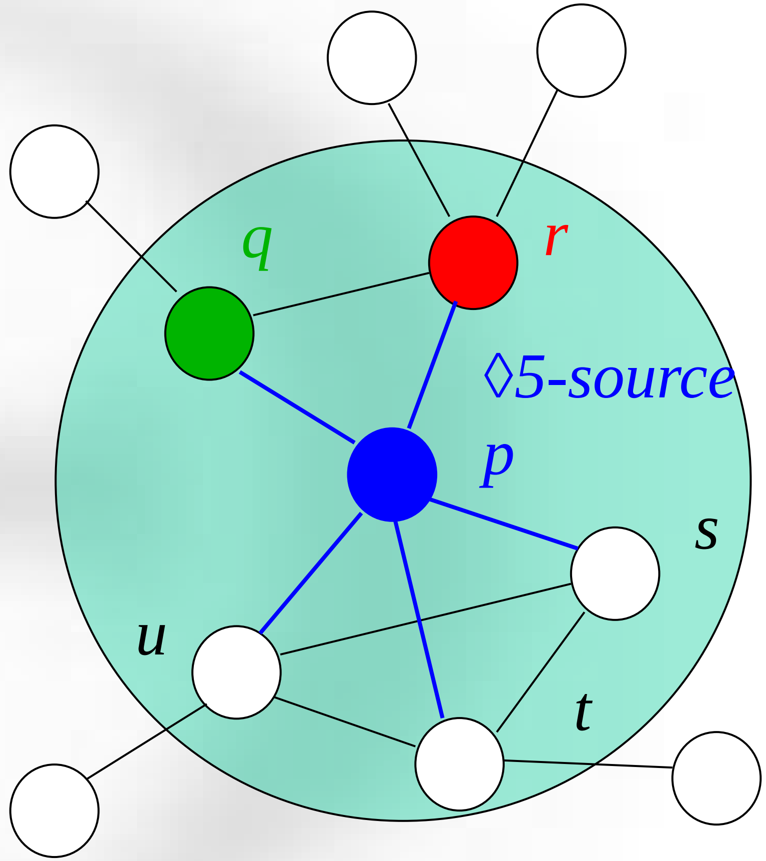
Aguilera, Delporte, Fauconnier, Toueg [ADFT04], Hutle, Malkhi, Schmid, Zhou [HMSZ09]:

- Partially synchronous processors (Φ) with crash failures
- Almost all communication asynchronous, except:
- At least one process *p* must be an $\Diamond f$-source:
  - After some (unknown) time, *p* has timely links to at least *f* neighbors [*No message sent at time t is processed after* $t+\tau^+$ *(unknown)*]
  - Note: A link to a crashed process is timely per definition!
- Allows to implement Ω, and hence solving consensus for $n > 2f$
- An $\Diamond f$-1-source is provably not sufficient
- Currently weakest WTL model [HMSZ09]: A moving $\Diamond f$-source, where the *f* timely links can change with time

Weak Timely Link Models (II)

Ω implementation: Every process

- periodically broadcasts heartbeat message (HB)
- times-out HBs of all neighbors
  - using weak local clock [implemented via step counting in spin-loop]
  - timeout value increased on every TO [= no HB received before expiration]
- broadcasts accusation message *acmsg*(*q*) on every TO for *q*'s HB
- if *n*-*f* *acmsg*(*q*) are received, then increment *acc_count*[*q*]
- Ω-output: *q* with min. *acc_count*[*q*]



- All processes accuse crashed r → *acc_count*[*r*] continuously grows
- 5+1 processes never accuse p → incrementing *acc_count*[*p*] stops

Even Weaker ParSync Models?

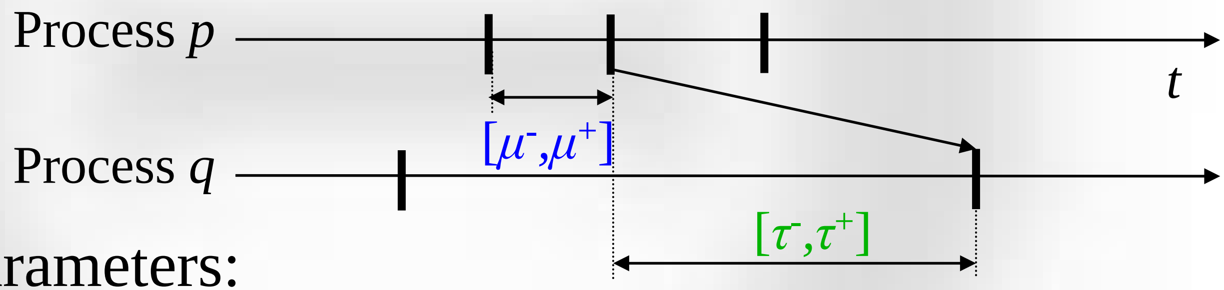
- Investigate models for weaker problems, like *k*-set consensus [Cha93]
  - Biely, Robinson & Schmid [BRS09]: Weak ParSync models
  - Gafni & Kouznetsov [GK09]: Weakest FD
- Open major challenge:

How to quantify and compare the assumption coverage of ParSync models in real systems?

Distributed Real-Time Systems

Recall Classic DC Modeling and Analysis

- Processors/processes modeled as interacting state machines
- **Zero-time** atomic computing steps, usually time-triggered
  - Message Passing (MP): [receive] + compute + [send]
  - Shared Memory (SHM): [accessSHM] + compute

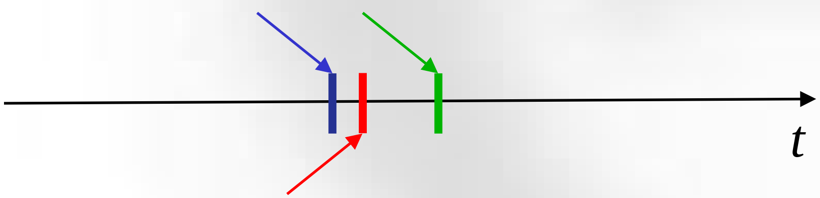


- System timing parameters:
  - Operation durations modeled via **inter-step times $[\mu^-,\mu^+]$** (often $\mu^- = 0$)
  - Message delays modeled as **end-to-end delays $[\tau^-, \tau^+]$** (often $\tau^- = 0$)
- DC research established a wealth of results:
  - Correctness proofs of distributed algorithms
  - Impossibility & lower bound results

Real-Time Properties ?

Classic modeling:

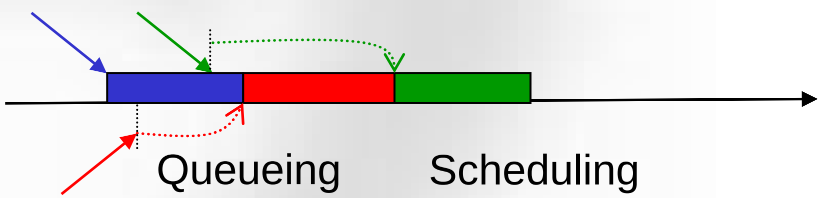
- $[\mu^-,\mu^+]$, $[\tau^-,\tau^+]$ are *a priori given* system parameters (alg-indep.)
- Analysis considers occurrence times of steps independently of each other:



- No queueing & scheduling in the picture
- Too optimistic time complexity

Reality:

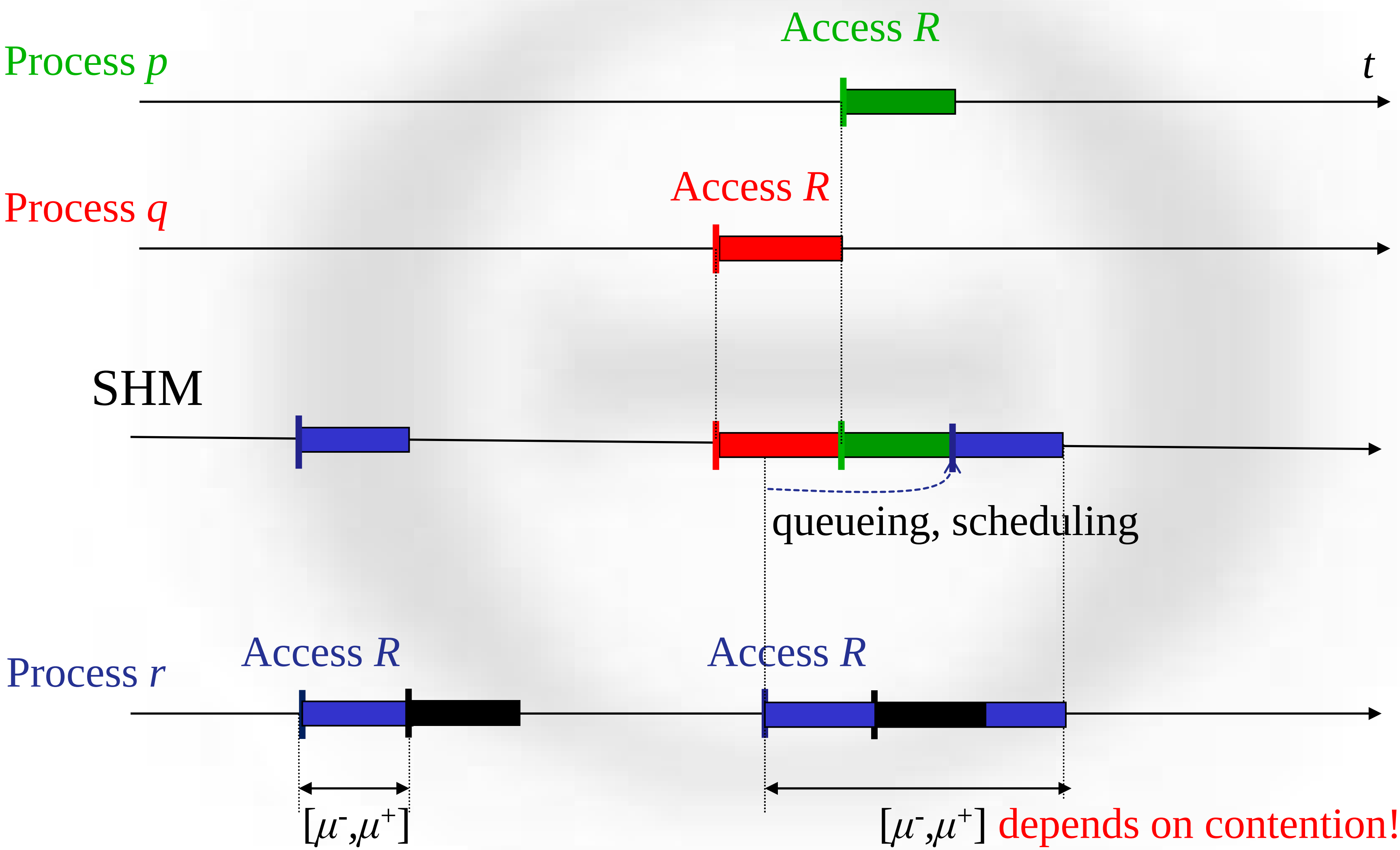
- $[\mu^-,\mu^+]$, $[\tau^-,\tau^+]$ depend on algorithms + scheduling policies
- Non-preemptible operations → steps not independent:



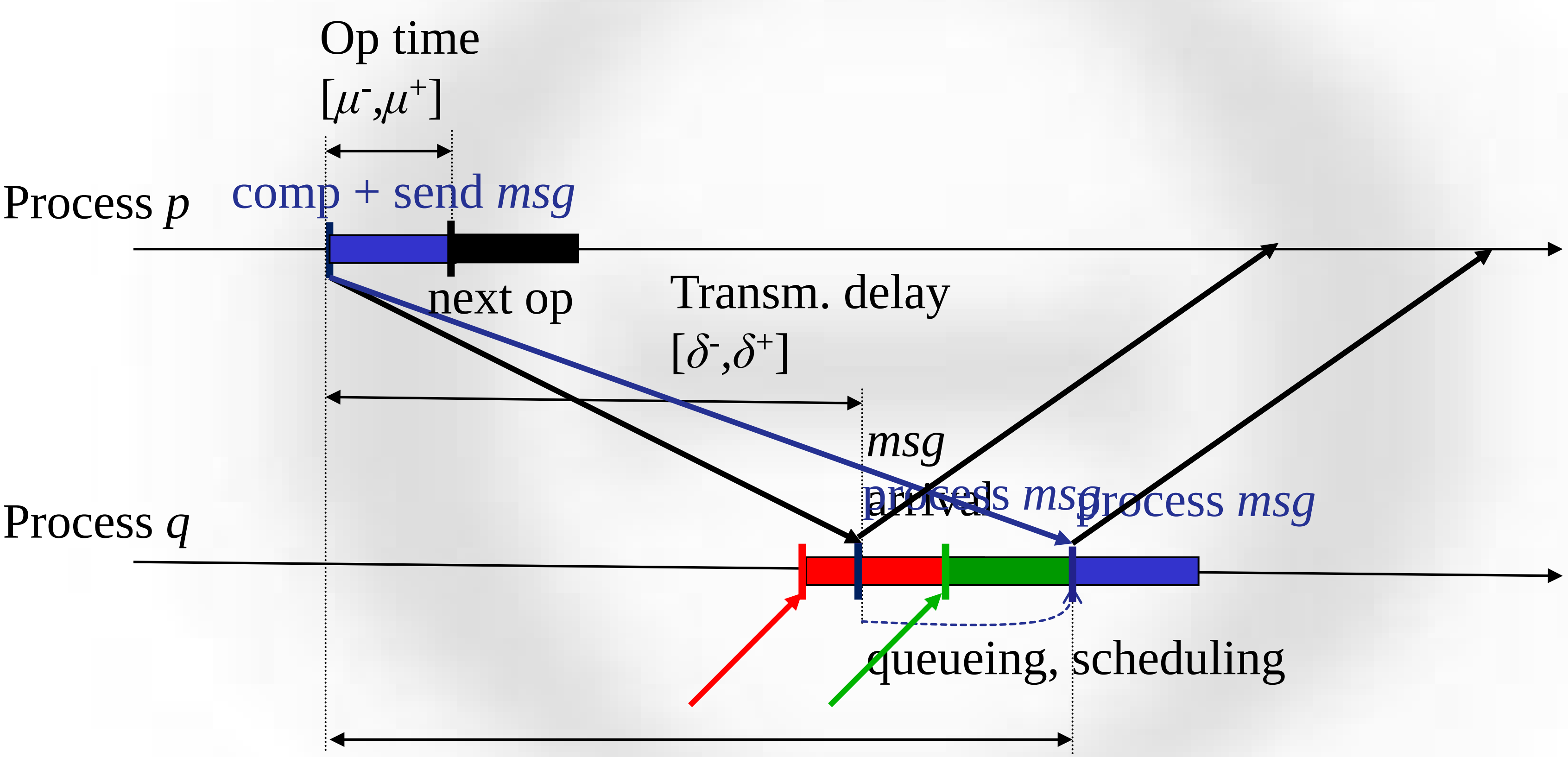
- Time complexity analysis involves real-time analysis

✓ Moser & Schmid [MS06,MS08]

Fixed Step Times in SHM Systems ?



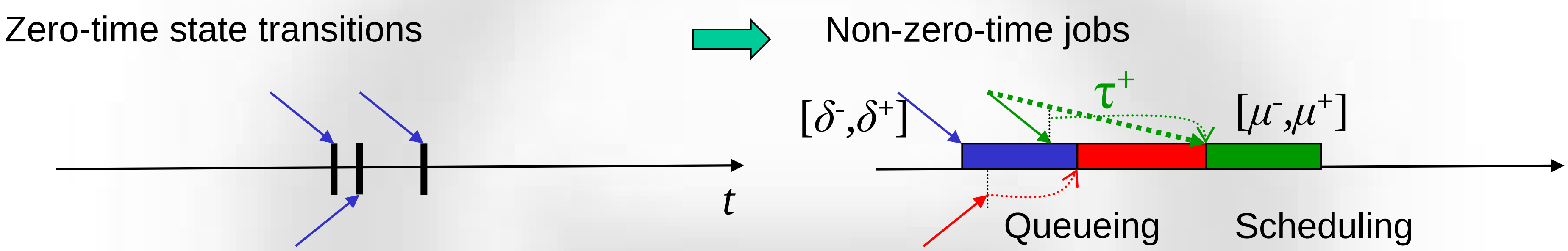
Fixed End-to-End Delays in MP Systems ?



E-t-e delay [τ^-, τ^+] depends on receiver load!

Real-Time Distributed Computing Model

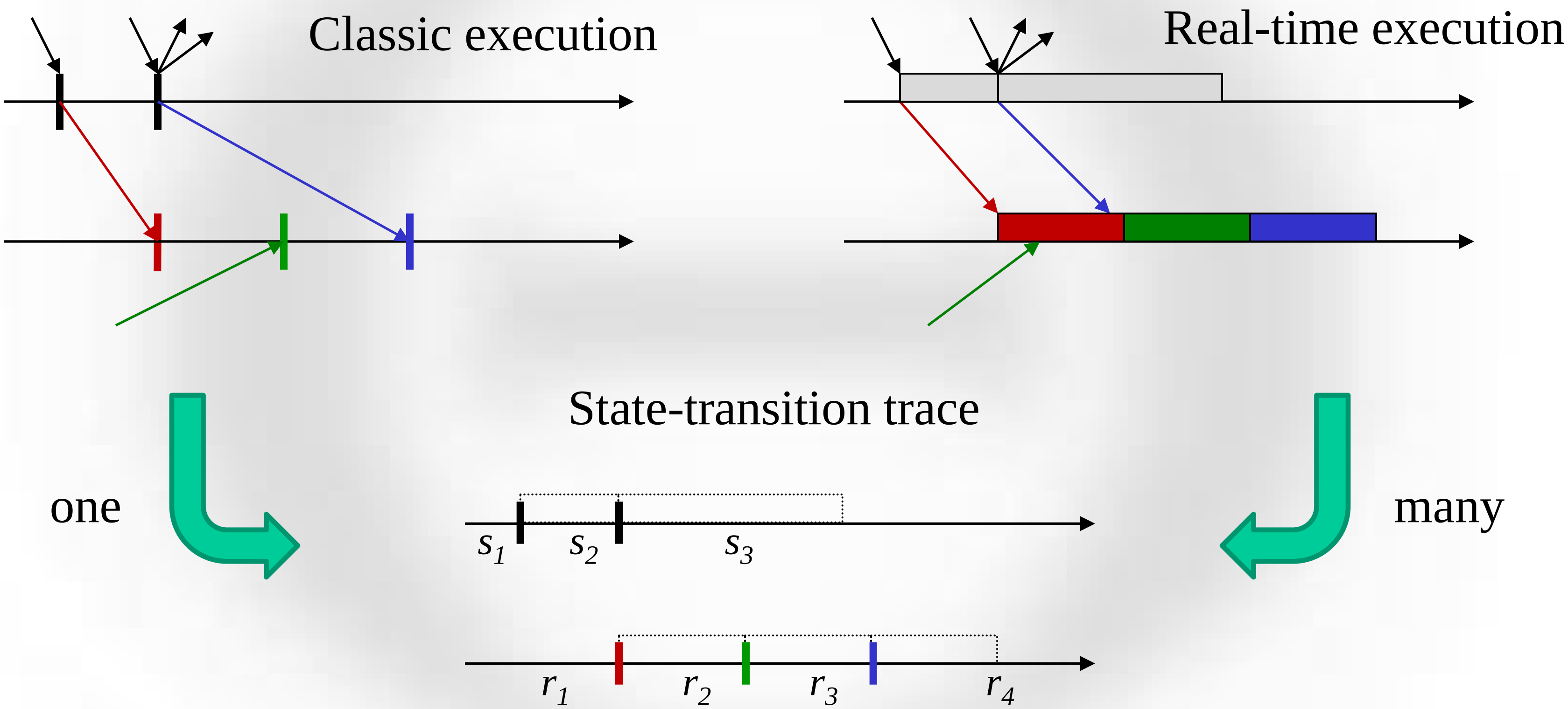
- RT model core features [Moser & Schmid, OPODIS'06]



- Investigate relation classic vs. RT model
  - Carry over classic failure models ?
  - Carry over classic correctness proofs ?
  - Carry over classic time complexity results ?
  - Carry over classic impossibility & lower bound results ?
- Conduct real-time analysis for e-t-e delays τ^+

State-Transition Problems

Can be defined for both models in the same way:



State-transition problem = a set of state-transition traces

Example: Problem Definition

Deterministic Drift-Free Clock Synchronization

$is\_finalstate(g) :\Leftrightarrow \forall g' \succ g : \forall p : s_p(g) = s_p(g')$

Termination: All processors eventually terminate.

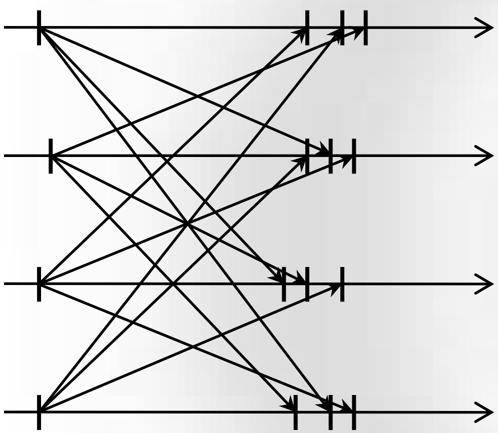
$\exists g : is\_finalstate(g)$

Agreement: After all processors have terminated, all processors have adjusted clocks within γ of each other.

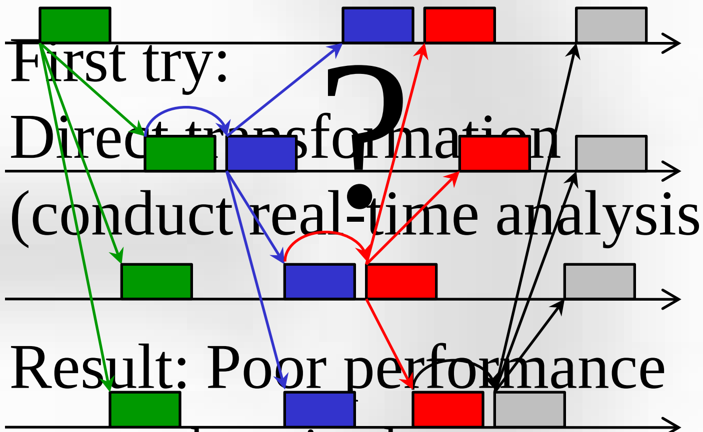
$\forall g : is\_finalstate(g) \Rightarrow (\forall p, q : |AC_p(g) - AC_q(g)| \leq \gamma)$

Example: Drift-Free Clock Sync

Classic Model:



Real-time Model:



First try:

Direct transformation

(conduct real-time analysis)

Result: Poor performance

- sub-optimal worst-case precision
- O(n) time

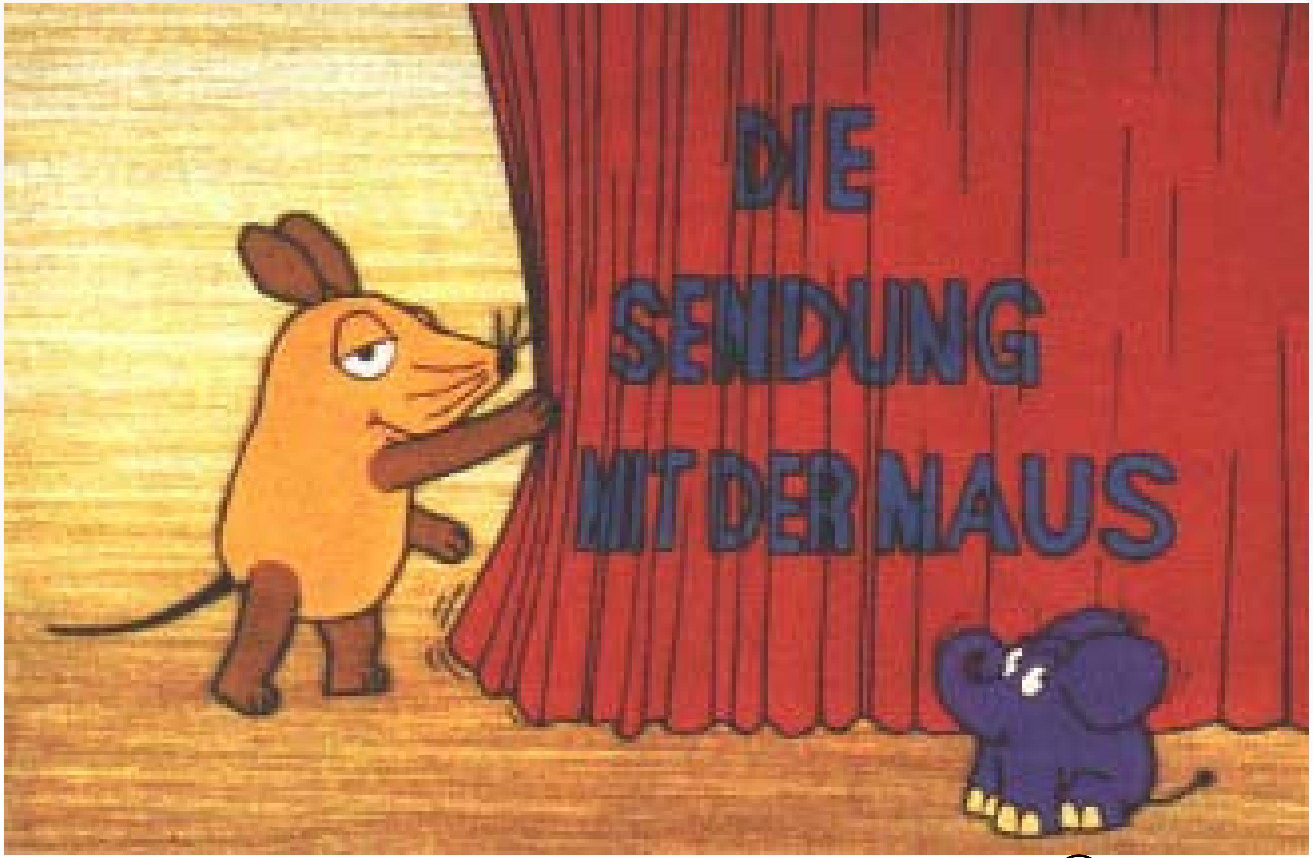
Result:

- Optimal worst-case precision
- Optimal running time O(1)

Result:

- Optimal worst-case precision
- Achievable only in time O(n)
- O(1) time algorithm with sub-optimal precision also exists

The End
(Part 2)



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